Wafer-scale high-density edge coupling for high throughput testing of silicon photonics

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Abstract: High-throughput functional testing of silicon photonics is a key challenge for scalable manufacturing. We present a technique for wafer-scale testing using high-density edge couplers that add excess loss of $<$2.2dB without requiring additional footprint.

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1. Introduction

The shift in silicon photonics from the development of components and sub-systems to the production of standalone products has yielded many platform-specific, power efficient techniques for coupling, packaging, and testing. Presently, a large majority of silicon photonic systems rely on edge coupling or grating coupling. The most efficient power coupling scheme is through the implementation of inverse tapers in edge couplers [1]. These structures achieve ultra-low coupling losses of 0.25 dB at an optical 3 dB bandwidth of 300 nm and low a polarization dependent loss (PDL). Conversely, grating couplers [2] demonstrate higher coupling loss (in the range of 4.5 dB), have an optical 3 dB bandwidth of merely 50 nm, and ordinarily only operate efficiently for one polarization. However, grating couplers possess two important advantages over edge couplers: 1) the possibility to couple modes from cleaved fibers, and 2) the fact that light couples nearly vertically into the chip, which enables wafer-scale device testing. Currently, the resources needed to test and package a silicon photonic system exceed its fabrication costs [3]. To reduce test costs, wafer-scale testing is needed as it reduces the overall production cost several ways. Firstly, wafer-scale coupling enables inline control testing, which allows for the monitoring of the health of the process line. Secondly, loading a single wafer with hundreds of devices is much faster than pick and place every device separately. Finally, if a wafer does not meet specifications, fabrication can be aborted early in the production process, which saves packaging resources. In this paper, we present a new technique that facilitates the coupling and testing of edge couplers on a wafer scale; an approach that combines the low-loss characteristics of edge couplers with the versatility of grating couplers.

2. Coupling Concept

In the final etch step of chip fabrication, the dicing channels are engraved to superficially divide the individual chips on a wafer. For wafer disks containing photonic chips, an extra step is taken to broaden the trenches in order to create clean etched facets for better edge coupling results. Because the actual chip dicing step is performed using a dicing saw, the opened dicing lanes will be around 200 μm wide. The trench depth does not need to be perfectly controlled and will exceed several 10th of μm in most cases.

To couple light into the edge couplers, we take advantage of these dicing lanes. The idea is to send light downwards into the trench, and then deflect it into the coupler. Following the development of quasi-planar coupling [4] for grating couplers, our novel approach utilizes a planar lightwave circuit (PLC) as an optical probe by inserting it vertically into a dicing channel next to edge couplers. The channel-facing end of the PLC is cleaved at an angle, so that light guided downwards through the PLC will deflect off the angled wall via total internal reflection and enter a coupler (Figure 1).

The advantages of our coupling technique builds upon all the benefits of using a fiber array. If the PLC were designed to have a multitude of channels, parallel coupling of many I/Os can be realized, as it is currently with fiber arrays. The advantage of using the PLC is that it would be coupling to edge couplers, and thus would be less susceptible loss when compared to the fiber arrays which couple to grating couplers. In addition, the PLC optical probe is monolithic, enabling easy handling and manipulation. The clear geometric features of the proposed probe allows for the application of machine vision techniques for automation of the coupling process. Furthermore, since PLCs are fabricated in silica, they have a much wider optical bandwidth than the bandwidth of the devices under test. Lastly, our approach is

polarization and wavelength independent, as the main mechanism of the coupling concept is total internal reflection. Other advantages include the possibility of tailoring the waveguides [4] to the mode required by the edge coupler, and using the device to increase I/O density for testing.

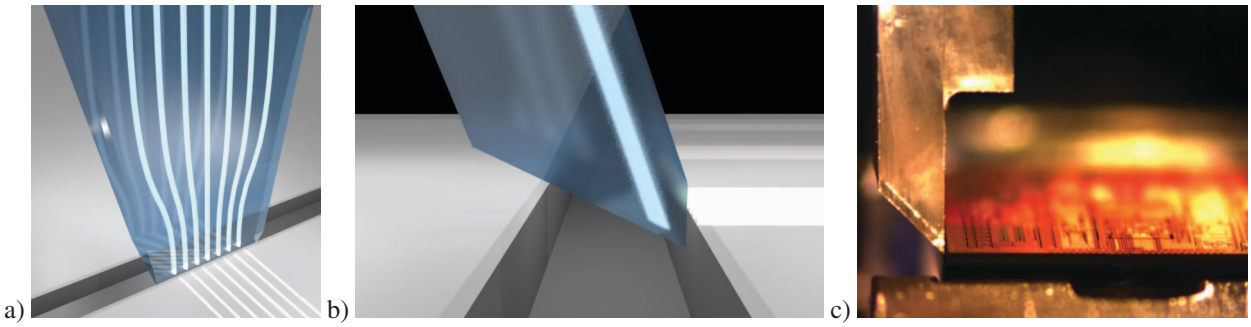

Fig. 1. a) Frontal view of the proposed optical probe for wafer-scale edge coupling, b) Lateral view of the coupling principle based on trenches in the wafer and a planar lightwave circuit (PLC), c) An image of the prototypical optical probe coupling to a characterization chip.

3. Measurement Results

To assess the validity of our idea, we bought an off-the-shelf planar lightwave circuit originally purposed for quasi-planar coupling of grating couplers to use as our optical probe. The PLC (Figure 1.c) contains straight waveguides in a silica glass substrate. The glass substrate itself is optimized for minimal coupling loss from single mode fibers (SMF) to the PLC. The waveguides' dimensions are 9 µm by 9 µm, and have a refractive index 0.3% higher than the glass substrate. These waveguides are located 20 µm deep in the substrate. The tip of the PLC has been polished to a 45° angle, and a v-groove fiber array is used to connect single mode fibers to the body of the PLC. This optical probe has a measured total injection loss of 1.5 dB which splits into:

	FC/APC Connector	SMF to PLC	Waveguide	Total internal reflection	Silica Air Interface
Loss [dB]	0.2	0.3	0.1	0.6	0.3

Note that some loss is due to beam components having an incident angle lower than the critical angle, 43°, for the total internal reflection on a silica air interface. The numerical aperture of the waveguide allows for incident angles of around 5°, which leads to light components being transmitted through the interface. This loss component can be reduced by increasing the reflection angle.

We used a manual 6 axis stage to couple the optical probe to a cleaved single mode fiber as well as to a silicon photonic chip fabricated by AIM Photonics. The characterization structure on-chip is a simple loop-back in the silicon nitrite layer. AIM Photonics' standard edge couplers were used in this experiment, which were optimized for coupling with cleaved single mode fiber (Figure 2.a).

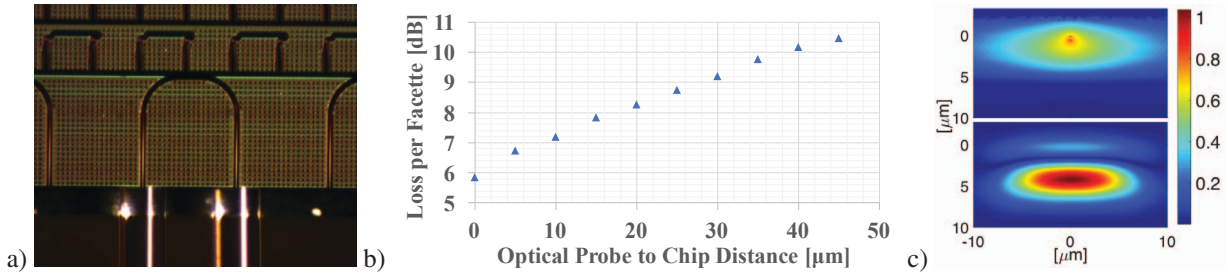

Fig. 2. a) Shows the used test structure coupled by single mode fiber, b) Depicts the dependence of the loss on the distance between probe and the chip facet c) Mode field distribution of edge coupler (top) and optimized optical probe (bottom).

A total insertion loss of 3.3 dB was measured when coupling the optical probe to a single mode fiber. The increased loss is attributed to the passing of light through the 20 µm cladding, resulting in an expansion of the mode which leads to less light being coupled into the single mode fiber. The measured PDL is an expected minimum of 0.3 dB. When the optical probe was coupled to the chip, a total loss per facet of 5.7 dB was measured. This corresponds to an excess loss of only 2.2 dB compared to measurements performed using single mode fibers coupling the same chip. The PDL of silicon nitrite waveguides is naturally high, we observed an unexpected increase of 2 dB per facet in PDL(Table 1). The loss dependence on the distance between optical fiber and the chip is shown in Figure 2.b. Note that at a reasonable working distance of 10 µm the excess loss is still only 3.6 dB.

Table 1. Characterization Results

	Optical Probe to SMF	SMF to Chip	Optical Probe to Chip	**Excess Loss**
Loss per Facet [dB]	3.3	3.5	5.7	**2.2**
PDL [dB]	0.3	9.5	11.5	**2.0**

4. Design Optimization

As this technique was developed to enable high throughput testing of silicon photonic chips, the optical probe must be designed to allow for automated coupling using machine vision systems. Most automated probing systems rely on one top-view camera. The current design of the PLC obstructs the top view, as can be seen in Figure 1.c . This implies that the optical probe should ideally to be tilted backwards (Figure 1.b). The tilt not only assists with automated coupling, but it also reduces the loss on the total internal reflection interface. For a 100 µm deep and 100 µm wide trench, the reflection angle can be easily widened from 90° to 120°. As mentioned in Section 3, the waveguides are buried 20 µm in the substrate, which leads to significant divergence of the beam inside the optical probe upon deflection. Thinning the substrate therefore leads to further reduction of coupling loss due to a reduced mode mismatch between the optical probe and the edge coupler. Finally, the waveguides of the PLC are currently optimized for minimal coupling loss to single mode fibers. Therefore, mode matching between optical probe and edge coupler can be further improved by optimizing waveguides on the probe's output and by including an adiabatically tapered waveguide to the probe's input.

A finite-difference time-domain simulation-based optimization of the structure results in a design with a reflection angle of 120°, a reduced waveguide depth of 14 µm, and a waveguide geometry of 12 µm by 10.5 µm. This optimized geometry produces a mode that matches the mode of the simulated edge coupler to 95.9% (Figure 2.c). For reference, the original, off-the-counter design only achieves a mode match of 73.4% . Including all other known losses, e.g. fiber coupler loss, waveguide loss, etc. we compute a total coupling loss of less than 1.5 dB.

5. Conclusion

We have demonstrated a new testing method to enable wafer-scale testing of edge couplers. Our approach introduces a PLC-based optical probe into the dicing trenches of silicon wafers to couple light into the edge couplers of photonic chips prior to dicing. Measurements taken using an off-the-shelf product shows an excess losses of only 2.2 dB compared to optimal coupling with a cleaved fiber. Furthermore, we discussed ways to reduce the total coupling loss to less than 1.5 dB and make the device ready for usage in an automated probing system. The approach has no overhead in footprint, allows parallel testing, and has low loss. Hence, the proposed technique enables low cost, high-throughput testing of photonic devices in fabrication.

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